IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently amended): A logic apparatus comprising:

a semiconductor substrate;

a first single-electron device comprising,

a first conductive island insulatively disposed over the semiconductor substrate,

at least two first tunnel barriers insulatively disposed over the semiconductor substrate, the first conductive island being interposed between the first tunnel barriers,

first and second electrodes insulatively disposed over the semiconductor substrate, the first conductive island being coupled with the first and second electrodes through the first tunnel barriers, respectively, and

a first charge storage region insulatively disposed over the first conductive island; [[and]]

a second single-electron device comprising,

a second conductive island insulatively disposed over the semiconductor substrate,

at least two second tunnel barriers insulatively disposed over the semiconductor substrate, the second conductive island being interposed between the second tunnel barriers,

third and fourth electrodes insulatively disposed over the semiconductor substrate, the second conductive island being coupled with the third and fourth electrodes through the second tunnel barriers, respectively, and

a second charge storage region insulatively disposed over the second conductive island[[,]] ; and

a connection between the third electrode of the ~~second single-electron~~ second single-electron device ~~being connected to~~ and the first electrode of the first single-electron device,

wherein, for each of the first and second single-electron devices, a Coulomb oscillation in a state that charges are accumulated in the charge storage region is shifted by a half-period from the Coulomb oscillation in a state that no charge is accumulated therein.

Claim 2 (Currently Amended): A logic apparatus according to claim 1, ~~which includes~~ further comprising an output amplifier connected to the first electrode of the first single-electron device and the third electrode of the second single-electron device.

Claim 3 (Currently Amended): A logic apparatus according to claim 1, wherein the first and second single-electron devices include fifth and sixth electrodes insulatively disposed over the first and second charge storage regions, respectively, [[and]] logic signals are input to the fifth and sixth electrodes of the first and second single-electron devices, and a logic operation result is output from the first and third electrodes.

Claim 4 (Original): A logic apparatus according to claim 3, wherein the first electrode and the third electrode are formed of a common electrode region.

Claim 5 (Currently Amended): A logic apparatus according to claim 1, wherein the first and second single-electron devices include fifth and sixth electrodes insulatively disposed over the first and second charge storage regions, respectively, logic signals are input

to the fifth and the sixth electrode of the first and the second single-electron device, and a logic operation result is output from the second electrode of the first single-electron device.

Claim 6 (Original): A logic apparatus according to claim 5, wherein the first electrode and the third electrode are formed of a common electrode region.

Claim 7 (Currently Amended): A logic apparatus according to claim 1, wherein each of the first and second single-electron devices has a ~~logical~~ logic inversion relation between a state that charges are accumulated in the charge storage region and a state that no charge is accumulated therein.

Claim 8 (Currently Amended): A logic apparatus according to claim 1, ~~which includes~~ wherein each of the first and second single-electron devices further comprises an element configured to inject charges to the charge storage region or extract charges therefrom.

Claim 9 (Currently Amended): A logic apparatus according to claim 1, ~~which~~ wherein each of the first and second single-electron devices further comprises an element configured to generate a potential difference between the conductive island and the charge storage ~~regions~~ region, in order to inject charges to the charge storage region or extract charges therefrom.

Claim 10 (Canceled).

Claim 11 (Currently amended): A logic apparatus according to claim [[10]] 1, wherein, for each of the first and second single-electron devices, a size and materials of the conductive island are selectively set to shift the Coulomb oscillation by [[a]] the ~~half-period~~ half-period between [[a]] the state that charges are accumulated in the charge storage region and [[a]] the state that no charge is accumulated therein.

Claim 12 (Currently Amended): ~~A logic apparatus according to claim 1, which includes~~ A logic apparatus comprising:

a semiconductor substrate;

a first single-electron device comprising,

a first conductive island insulatively disposed over the semiconductor substrate,

at least two first tunnel barriers insulatively disposed over the semiconductor substrate, the first conductive island being interposed between the first tunnel barriers,

first and second electrodes insulatively disposed over the semiconductor substrate, the first conductive island being coupled with the first and second electrodes through the first tunnel barriers, respectively, and

a first charge storage region insulatively disposed over the first conductive island;

a second single-electron device comprising,

a second conductive island insulatively disposed over the semiconductor substrate,

at least two second tunnel barriers insulatively disposed over the semiconductor substrate, the second conductive island being interposed between the second tunnel barriers,

third and fourth electrodes insulatively disposed over the semiconductor substrate, the second conductive island being coupled with the third and fourth electrodes through the second tunnel barriers, respectively, and

a second charge storage region insulatively disposed over the second conductive island; and

a connection between the third electrode of the second single-electron device and the first electrode of the first single-electron device;

a resistor between a node of the first electrode of the first single-electron device, [[and]] the third electrode of the second single-electron device, and a voltage source; and

~~wherein~~ at least one ground terminal connected to the second electrode of the first single-electron device and the fourth electrode of the second single-electron device ~~are grounded~~.

Claim 13 (Currently Amended): A logic apparatus according to claim 1, further comprising a plurality of single-electron device pairs each including the first and second single-electron devices ~~according to claim 1, the first and second single-electron device pairs being~~ connected in parallel or serial.

Claim 14 (Currently Amended): A logic apparatus according to claim 1, further comprising a plurality of single-electron device pairs each including the first and second single-electron devices ~~according to claim 1, the first and second single-electron device pairs being~~ connected in parallel and serial.

Claim 15 (Currently Amended): A logic circuit comprising:

a first logic circuit using a single-electron device ~~occurring~~ having an oscillation according to a voltage, ~~and having~~ a capacitor configured to selectively store charges, a first terminal, a second terminal, and a third terminal;

a second logic circuit using a single-electron device ~~occurring~~ having an oscillation according to a voltage, ~~and having~~ a capacitor configured to selectively store charges, a first terminal connected to the first terminal of the first logic circuit, a second terminal, and a third terminal;

a resistor connected to a node of the first terminals of the first and second logic circuits and a voltage source;

a ground terminal connected to the second terminals of the first and second logic circuits; and

~~logical~~ logic signal input terminals, connected to the third terminals of the first and second logic circuits, [[to be]] inputted with ~~logical~~ logic signals.

Claim 16 (Currently Amended): A logic circuit according to claim 15, ~~which includes~~ further comprising an output amplifier connected to the node of the first terminals of the first and second logic circuit.

Claim 17 (Original): A logic circuit according to claim 15, wherein a logic operation result is output from the first terminals of the first and second logic circuits.

Claim 18 (Original): A logic circuit according to claim 15, wherein a logic operation result is output from the second terminal of the first logic circuit.

Claim 19 (Currently Amended): A logic circuit according to claim 15, wherein each of the first and second logic circuits has a ~~logical~~ logic inversion relation between a state that charges are accumulated in the capacitor and a state that no charge is accumulated therein.

Claim 20 (Currently Amended): A logic circuit according to claim 15, ~~which includes~~ further comprising a circuit configured to inject charges to the capacitor or extract charges therefrom.

Claim 21 (Currently Amended): A logic circuit according to claim 15, further comprising a plurality of logic circuit pairs each including the first and second logic circuits ~~according to claim 15, the first and second logic circuits being~~ connected in parallel or serial.

Claim 22 (Currently Amended): A logic circuit according to claim 15, further comprising a plurality of logic circuit pairs each including the first and second logic circuits ~~according to claim 15, the first and second logic circuits being~~ connected in parallel and serial.

Claim 23 (New): A logic apparatus comprising:

a semiconductor substrate;

a first single-electron device comprising,

a first conductive island insulatively disposed over the semiconductor substrate,

at least two first tunnel barriers insulatively disposed over the semiconductor substrate, the first conductive island being interposed between the first tunnel barriers,

first and second electrodes insulatively disposed over the semiconductor substrate, the first conductive island being coupled with the first and second electrodes through the first tunnel barriers, respectively, and

a first means for storing charges to vary an energy state of the first conductive island;

a second single-electron device comprising,

a second conductive island insulatively disposed over the semiconductor substrate,

at least two second tunnel barriers insulatively disposed over the semiconductor substrate, the second conductive island being interposed between the second tunnel barriers,

third and fourth electrodes insulatively disposed over the semiconductor substrate, the second conductive island being coupled with the third and fourth electrodes through the second tunnel barriers, respectively, and

a second means for storing charges to vary an energy state of the second conductive island; and

a connection between the third electrode of the second-single electron device and the first electrode of the first single-electron device,

wherein, for each of the first and second single-electron devices, a Coulomb oscillation in a state that charges are accumulated in the means for storing charges is shifted by a half-period from the Coulomb oscillation in a state that no charge is accumulated therein.

Claim 24 (New): A logic apparatus according to claim 23, wherein the first and second single-electron devices include fifth and sixth electrodes insulatively disposed over the first and second means for storing charges, respectively, logic signals are input to the fifth and sixth electrodes of the first and second single-electron devices, and a logic operation result is output from the first and third electrodes.

Claim 25 (New): A logic apparatus according to claim 23, wherein the first and second single-electron devices include fifth and sixth electrodes insulatively disposed over the first and second means for storing charges, respectively, logic signals are input to the fifth and sixth electrode of the first and second single-electron device, and a logic operation result is output from the second electrode of the first single-electron device.

Claim 26 (New): A logic apparatus according to claim 23, wherein each of the first and second single-electron devices has a logic inversion relation between a state that charges are accumulated in the means for storing charges and a state that no charge is accumulated therein.

Claim 27 (New): A logic apparatus comprising:

a semiconductor substrate;

a first single-electron device comprising,

a first conductive island insulatively disposed over the semiconductor substrate,

at least two first tunnel barriers insulatively disposed over the semiconductor substrate, the first conductive island being interposed between the first tunnel barriers,

first and second electrodes insulatively disposed over the semiconductor substrate, the first conductive island being coupled with the first and second electrodes through the first tunnel barriers, respectively, and

a first means for storing charges to vary an energy state of the first conductive island;

a second single-electron device comprising,

a second conductive island insulatively disposed over the semiconductor substrate,

at least two second tunnel barriers insulatively disposed over the semiconductor substrate, the second conductive island being interposed between the second tunnel barriers,

third and fourth electrodes insulatively disposed over the semiconductor substrate, the second conductive island being coupled with the third and fourth electrodes through the second tunnel barriers, respectively, and

a second means for storing charges to vary an energy state of the second conductive island;

a connection between the third electrode of the second-single electron device and the first electrode of the first single-electron device;

a resistor between a node of the first electrode of the first single-electron device, the third electrode of the second single-electron device, and a voltage source; and

at least one ground terminal connected to the second electrode of the first single-electron device and the fourth electrode of the second single-electron device.